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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,240	02/06/2004	Soon-Kyun Shin	9862-000023/US	6620

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,240	SHIN, SOON-KYUN	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10-29 and 32* is/are rejected.

7)☒ Claim(s) *5-9,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 06/28/05. A new ground of rejection is introduced as necessitated by amendment.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1- rejected under 35 U.S.C. 102(b) as being anticipated by Bayer et al. (USP 6392904).

As to clamp 1, Bayer et al. discloses in figure 1 an apparatus for controlling a boosted voltage comprising: a voltage generating circuit configured to generate a boosted voltage (Vout) from an input voltage (Vin) based on a control current (4) and charges stored in a charge storing element (Cpump), and configured to receive the control current while the charges stored in the charge storing element are used to generate the boosted voltage; and a control circuit (R1, R2, 5, 3) configured to generate the control current based on the boosted voltage.

As to claim 2, figure 1 shows the voltage generating circuit comprises: a capacitor (Cpump); and a switching structure configured to selectively store charges corresponding to the input voltage in the capacitor, and to selectively output the stored charges in conjunction with charges corresponding to the control current as the boosted voltage.

As to claim 3, figure 1 shows the control circuit is configured to generate the control current based on a difference between the boosted voltage and a desired boosted voltage (Vref).

As to claim 4, figure 1 shows that the voltage generating circuit comprises: first, second, third and fourth switches (S1-S4); and a capacitor configured to store charges corresponding to the input voltage while the second and third switches are turned on, and outputting the boosted voltage while the first and fourth switches are turned on.

As to claim 10, figure 1 shows that the control circuit is configured to generate the control current based on the boosted voltage and a desired boosted voltage.

As to claim 11, figure 1 shows that the control circuit is configured to generate the control current based on a difference between the boosted voltage mad the desired boosted voltage.

As to claim 12, figure 1 shows that the control circuit comprises a voltage divider (R1, R2) configured to generate a divided voltage from the boosted voltage; a comparator (5) configured to compare the divided voltage with a reference voltage (Vref); and a current generator (4) configured to generate the control current based on output from the comparator.

As to claim 13, figure 1 shows that the reference voltage represents a desired boosted voltage.

As to claim 14, figure 1 shows that the control circuit comprises: a voltage divider (R1, R2) configured to divide the boosted voltage to generate a divided voltage, an amplifier (5) configured to amplify a difference voltage between a reference voltage and the divided voltage; and a voltage controlled current source (4) configured to generate the control current based on the amplified difference voltage.

As to claim 15, figure 1 shows that the reference voltage represents a desired boosted voltage.

As to claim 17, figure 1 shows that voltage controlled current source decreases the control current when the divided voltage is higher than the reference voltage, and increases the control current when the divided voltage is lower than the reference voltage.

Claims 17-25 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claim 26, figure 1 shows that the switching structure is configured to selectively receive the control current while configured to selectively output the stored charges.

As to claim 27, figure 1 shows that the switching structure includes a switch configured to selectively connect a portion of the control circuit generating the control current with the capacitor.

As to claim 28, figure 1 shows that the voltage generating circuit is configured to not receive the control current when charges are stored in the capacitor.

As to claim 29, figure 1 shows that the first switch is configured to connect a portion of the control circuit generating the control current to the capacitor when turned on.

As to claim 32, figure 1 shows an apparatus for controlling a boosted voltage, comprising: a voltage generating circuit configured to generate a boosted voltage from an input voltage (Vin) based on a control current (4) and charges stored in a charge storing element (Pump); and a control circuit (R1, R2, 5, 3) configured to generate the control current based on the boosted voltage, and configured to supply the control current to the voltage generating circuit while the charges stored in the charge storing element are used to generate the boosted voltage.

Allowable Subject Matter

3. Claims 5-9, 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5-9, 30 and 31 would be allowable because the prior art fails to teach or suggest the voltage generator comprising the combination of clock generator and level shifter as claimed.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

July 25, 2005